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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,137	10/21/2003	David H. Asher	200301840-2	3633

7590 02/07/2007

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EXAMINER	
KIM, DANIEL Y	
ART UNIT	PAPER NUMBER
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,137	ASHER ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,13-15 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13-15 and 19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

STEPHEN C. ELMORE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION - 112 Second Paragraph (due to missing essential steps, elements, structure, between the elements of the claim)

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim a rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: xyz.

a. ;

b. ;

D 7-34 - 13, 12, 14

Claim a rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: xyz.

a. ;

b. ;

Claim a rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: xyz.

a.;

b. ;

DETAILED ACTION

Status

1. This Office Action is in response to applicant's communication filed November 10, 2006 in response to the PTO Office Action mailed August 10, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, no claims have been canceled, amended or added. Claims 1-9, 13-15 and 19-24 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-2, 6-7, 13-14, 19, 22 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the phrase "a fast access time" is relative and renders the claim indefinite. Specifically, the term "fast" makes the scope of what is meant by the claim language indefinite.

Claim 22 is rejected due to a similar reason, and should be corrected accordingly.

In claim 2, the phrases "a faster access time" and "a physically shorter path" are relative and render the claim indefinite. The terms "faster" and "shorter" are not fully defined by the claim. Specifically, it is unclear from the language how the "first way" provides "a faster access time" or a "physically shorter path", and what these concepts are with respect to. The language should be changed to include these concepts, in a manner such as "has a physically shorter path than any of the other first way segments".

Claims 7, 13-14 and 24 are rejected due to similar reasons, and should be corrected accordingly.

In claim 6, the phrase "proper control" is relative and renders the claim indefinite. The phrase is not clearly defined by the claim because it is unclear from the language what "proper" is with respect to.

Appropriate correction to the aforementioned claims is required.

6. Claims 1, 7 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap

between the elements. See MPEP § 2172.01. The omitted elements are described as follows:

In claim 1, the phrase "a first way has a fast access time" indicates a missing essential element necessary to accomplish said "fast access time". While applicant describes this element, namely, "one way will be physically closer to... the access control logic" in paragraphs [0023-0024] of the specification, there is nothing in the limitations themselves that describes accomplishing this claimed feature.

Claims 7 and 22 are rejected due to similar reasons, and should be corrected accordingly.

7. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are described as follows:

In claim 6, the phrase "proper control" indicates a missing relationship because it is unclear what structural elements work together to accomplish said "proper control of said muxes". While applicant describes a possible relationship in paragraphs [0024-0034] of the specification, there is nothing limitations themselves that describes accomplishing this claimed feature.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-5, 7-9, 13-15, 19-20 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt et al (US Patent No. 6,256,728) in view of Chudnovsky et al (US Patent No. 6,381,669).

For claim 1, Witt discloses a novel architecture for set associative cache, comprising:

a set associative cache having a plurality of ways wherein the ways are segmented into a plurality of banks and wherein a first way has a fast access time (in one particular embodiment, L1 D-cache is a 128 KB two way set associative cache employing 64 byte lines; L1 D-cache may be organized as, for example, 32 banks of cache memory per way, col. 12, lines 36-44);

access control logic which manages access to the cache and is coupled to said plurality of ways (fetch/scan unit includes a fetch control unit, a plurality of select next blocks, an instruction select multiplexor, an instruction scanner, etc... fetch control unit is coupled to L1 I-cache, L0 I-cache, col. 12, lines 59-66, col. 13, lines 1-);

a plurality of muxes coupled to said first way in each of said banks and coupled to said access control logic (control unit provides a set of selection signals to mux to select the set of run sections including the selected instructions, as well as the instruction pointers corresponding to the selected instructions, col. 30, lines 35-38; it is

noted that mux, while illustrated as a single mux for simplicity... may be implemented by any suitable parallel or cascaded set of multiplexors, col. 30, lines 31-34).

Witt fails to disclose the remaining claim limitations.

Chudnovsky, however, helps disclose the access control logic controls the mux in a bank to remap any defective way in a bank to the first way in that same bank (a remapping and scrambling system enables fault tolerant operation of a memory system and fault tolerant operation of multi-processor and multi-bank systems, col. 17, lines 47-50; once testing is performed and defective elements such as memory blocks, banks, or processing units are found, defect information is stored and used by remapping circuitry, col. 17, lines 64-67).

Witt and Chudnovsky are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include remapping defective ways in a bank to the first way of the bank using multiplexers because this would enable fault tolerant operation of the whole memory system and fault tolerant operation of multi-processor and multi-bank systems on-a-chip (col. 17, lines 48-50), as taught by Chudnovsky.

For claim 2, Witt and Chudnovsky disclose the invention as per rejection of claim 1 above.

Witt further helps disclose said first way has a faster access time because it has a physically shorter path to said access control logic (L0 I-cache is a high speed cache memory for storying instruction bytes; because L1 I-cache is large, the access time of

L1 I-cache may be large... L0 I-cache is comparably smaller than L1 I-cache, and hence may support a more rapid access time, col. 8, lines 30-37).

For claim 3, the combined teachings of Witt and Chudnovsky disclose the invention as per rejection of claim 1 above.

Chudnovsky further helps disclose self test logic coupled to said access control logic to test the cache for defects (this testing can be internal, using various state of the art approaches, such as a built-in-self-test, col. 17, lines 57-63).

For claim 4, the combined teachings of Witt and Chudnovsky disclose the invention as per rejection of claim 3 above.

Chudnovsky further helps disclose said self test logic tests the cache for defects on power up (both the testing and reprogramming can be done following boot procedures, col. 18, lines 11-15).

For claim 5, the combined teachings of Witt and Chudnovsky disclose the invention as per rejection of claim 3 above.

Chudnovsky further helps disclose said self test logic stores the location of defects in a status register (following boot procedures the software tests the memory and downloads the list of bad elements into a RAM or register, col. 18, lines 13-15).

Claim 7 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 8 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 9 is rejected using the same rationale as for the rejection of claim 1 above.

For claim 13, the combined teachings of Burger and Chudnovsky disclose the invention as per rejection of claim 1 above.

Witt further helps disclose a microprocessor die (a processor includes a predecode unit, an L-1 I-cache, an L0 I-cache, a fetch/scan unit, an instruction queue, etc..., col. 4, lines 29-33).

Claim 14 is rejected using the same rationale as for the rejections of claims 2 and 13 above.

Claim 15 is rejected using the same rationale as for the rejections of claims 9 and 14 above.

Claim 19 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 20 is rejected using the same rationale as for the rejections of claims 3 and 19 above.

Claim 22 is rejected using the same rationale as for the rejection of claim 19 above.

Claim 23 is rejected using the same rationale as for the rejections of claims 15 and 22 above.

Claim 24 is rejected using the same rationale as for the rejection of claim 13 above.

10. Claims 6 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt et al (US Patent No. 6,256,728) in view of Chudnovsky et al (US Patent No. 6,381,669) and further in view of Rowlands et al (US Patent No. 6,748,492).

For claim 6, the combined teachings of Witt and Chudnovsky disclose the invention as per rejection of claim 5 above.

These teachings fail to disclose the limitations of the current claim.

Rowlands, however, helps disclose said access control logic reads the location of defects in the cache from the status register to determine proper control of said muxes (a combination of direct access transactions and deterministic setting may be used to provide cache testing by using a direct access transaction to select a test way, then using a memory transaction which misses the cache to cause test data to be loaded into the test way; a subsequent direct access transaction may then read the data from the test way to check the test data for correct storage in the selected entry, and the tag information may be captured in a register within the cache, which may be read from the register and checked for accuracy, col. 2, lines 50-59; the tag register outputs the data stored therein to a mux; decoder provides the selection control to a mux, and selects the data from data memory; the decoder decodes the address of a transaction and, if the address is the address to which the tag register is mapped, the decoder selects the contents of the tag register via a mux, col. 11, lines 23-31).

Witt, Chudnovsky and Rowlands are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include reading the location of defects in a cache from the status register because defect information would allow for effiecient use by the remapping circuitry (col. 17, lines 66-67), as taught by Chudnovsky.

For claim 21, the combined teachings of Witt and Chudnovsky disclose the invention as per rejection of claim 19 above.

These teachings fail to disclose the limitations of the current claim.

Rowlands, however, helps disclose a step of disabling a way in a bank when that way is defective (a way is established as a way to be selected for eviction responsive to performing a transaction, col. 3, lines 20-22).

Citation of Pertinent Prior Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Crouch et al (US Patent No. 5,617,531) discloses a data processor having a built-in internal self test controller for testing a plurality of memories internal to the data processor.

Contact Information

12. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

1-30-07

STEPHEN C. ELMORE
PRIMARY EXAMINER